

# Laboratory 1

(Due date: **011**: September 20<sup>th</sup>, **005**: September 21<sup>st</sup>, **007**: September 22<sup>nd</sup>)

## OBJECTIVES

- ✓ Introduce VHDL Coding for FPGAs.
- ✓ Learn to write testbenches in VHDL.
- ✓ Learn the Xilinx FPGA Design Flow with the Vivado HL: Synthesis, Simulation, and Bitstream Generation.
- ✓ Learn how to assign FPGA I/O pins and download the bitstream on the Nexys™ A7-50T Board (or A7-100T).

## VHDL CODING

- ✓ Refer to the [Tutorial: VHDL for FPGAs](#) for a list of examples.

## NEXYS™ A7-50T FPGA TRAINER BOARD SETUP

- The Nexys A7-50T Board can receive power from the Digilent USB-JTAG Port (J6). Connect your Board to a computer via the USB cable. If it does not turn on, connect the power supply of the Board.
- Nexys A7-50T documentation: Available in [class website](#).

## FIRST ACTIVITY (100/100)

### DESIGN PROBLEM

- A doctoral student is defending his Dissertation. A 4-member committee is in charge of evaluating the work. The members vote to accept or reject the work. A simple majority vote is required. In case of a tie, the chair of the committee makes the final determination.
- We assign  $a, b, c, d$  to the vote of each committee member ( $a$  represents the vote of the chair of the committee), where '1' means accept, and '0' reject.
- Design a circuit that generates  $f = 1$  when the committee accepts the work, and  $f = 0$  if the work is rejected.  
The Boolean variables  $a, b, c, d$  are represented by 4 switches ('0': switch is OFF, '1': switch is ON).  
The Boolean variable  $f$  is represented by an LED ('1': LED is ON, '0': LED is OFF).

- ✓ Complete the truth table for this circuit: (5 pts)
- ✓ Derive (simplify if possible) the Boolean expression: (10 pts)

$f =$

a	b	c	d	f
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

## PROCEDURE

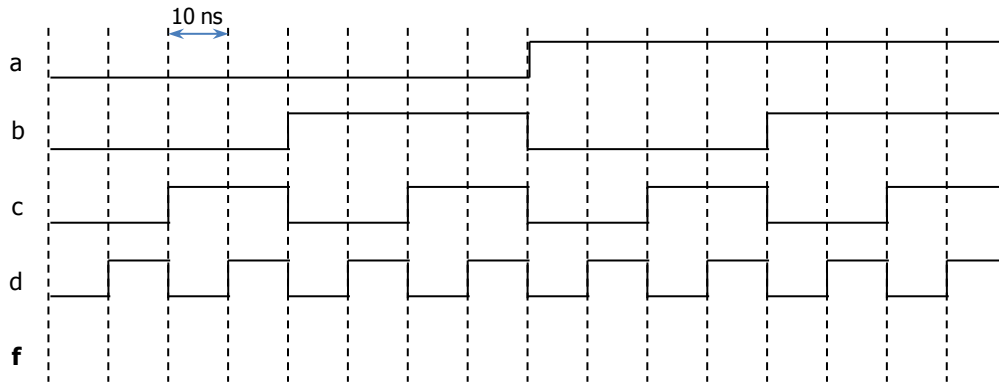
- **Vivado Design Flow for FPGAs: complete the following steps (follow the order strictly):** (85 pts)

- ✓ Create a new Vivado Project. Select the corresponding Artix-7 FPGA device as per the table:

Kit	Artix-7 FPGA Device	Master XDC File	Comments
Nexys A7-50T	XC7A50T-1CSG324I	Nexys-A7-50T-Master.xdc	Recommended board.
Nexys A7-100T	XC7A100T-1CSG324C	Nexys-A7-100T-Master.xdc	
Basys 3	XC7A35T-1CPG236C	Basys-3-Master.xdc	Suggested if you only take ECE2700
Nexys 4	XC7A100T-1CSG324C	Nexys4_Master.xdc	Discontinued
Nexys 4 DDR		Nexys4DDR_Master.xdc	

- ✓ Write the VHDL code that implements the simplified Boolean expression. Synthesize your circuit (Run Synthesis).

- ✓ Write the VHDL testbench to test every possible combination of the inputs.
  - The figure below provides a suggestion of what the input waveform described by your testbench should look like. Complete the output f so that you can compare it with the output generated by the simulator (next step).



- ✓ Perform Functional Simulation (Run Simulation → Run Behavioral Simulation). Verify that the output f generated by the simulator matches the one you manually completed. **Demonstrate this to your TA.**
- ✓ I/O Assignment: Generate the XDC file. Download the corresponding constraints file (XDC) of your board and edit it.
  - Use SW3, SW2, SW1, SW0 as inputs a, b, c, d respectively. Use LED0 as the output f.

Board pin names	SW3	SW2	SW1	SW0	LED0
Signal names in code	a	b	c	d	f

  - The board pin names (SW3–SW0, LED0) are used by all the listed boards (Nexys A7-50T/A7-100T, Basys 3, Nexys 4/DDR). The I/Os listed here are all active high.
- ✓ Implement your design (Run Implementation).
- ✓ Do Timing Simulation (Run Simulation → Run Post-Implementation Timing Simulation). **Demonstrate this to your TA.**
- ✓ Generate the bitstream file (Generate Bitstream).
- ✓ Download the bitstream on the FPGA (Open Hardware Manager) and test. **Demonstrate this to your TA.**

- Submit ([as a .pdf](#)) this lab sheet completed and signed off by the TA (or instructor)
- Submit ([as a .zip file](#)) the generated files: VHDL code, VHDL testbench, and XDC file to Moodle (an assignment will be created). DO NOT submit the whole Vivado Project.
  - ✓ Your .zip file should only include one folder. Do not include subdirectories.
    - It is strongly recommended that all your design files, testbench, and constraints file be located in a single directory. This will allow for a smooth experience with Vivado.
  - ✓ You should only submit your source files AFTER you have demoed your work. Submission of work files without demo will get NO CREDIT.

**lab1**

- top.vhd      Design file
- top\_tb.vhd    Testbench file
- lab1.xdc      Constraints file

TA signature: \_\_\_\_\_

Date: \_\_\_\_\_